UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,664	10/16/2001	Anthony Debling	S1022/8761	7581

23628 7590 02/25/2005

WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2211

EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,664	DEBLING, ANTHONY	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/16/01, 12/17/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 have been examined and claims 1-12 have been rejected.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file. The priority date is October 18, 2000.

Drawings

3. The drawings are objected to for the following reasons. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3-1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description:

(a) telephone line 761, as described in line 2 of page 10.

3-2. The reference sign 741 as shown in FIG. 3 should refer to the wiring between 750 and 740 as mentioned in line 10, page 9 of the specification.

Abstract

4. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old

apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

5. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said", should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns", "The disclosure defined by this invention", "The disclosure describes", etc.

6. The abstract of the disclosure is identical to claim 1. Therefore, the abstract is objected to because it is not in narrative form and uses legal phraseology, for example, "said". Correction is required. See MPEP § 608.01(b).

Claim Objections

7. Claim 1 is an independent device claim comprising a plurality of elements in the claim. Each element of a claim should be separated by a line indentation, 37 CFR 1.75(i). See MPEP § 608.01(m).

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 2-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9-1. Claim 2 recites the limitation "said chip" in line 2 of the claim. It is vague and indefinite regarding "said chip" because two different "chips", have been respectively recited at line 1, i.e., "a target integrated circuit chip", and line 6, i.e., "a further integrated circuit chip", of the claim.

9-2. Claim 3 recites the limitation "said universal serial bus" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

9-3. Claim 6 recites the limitation "The combination" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

9-4. Claims not specifically rejected above are rejected as being dependent on a rejected claim.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 9, 11, and 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Silverman et al., U.S. Patent 6,370,603 B1 issued April 9, 2002 and filed October 5, 1998.

11-1. Regarding claim 1, Silverman et al. disclose a communication device for a target integrated circuit chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry, and a target on-chip universal serial bus interface connected to said on-chip emulator, the communication device comprising an Ethernet port (Ethernet side 814, Figure 8A), a universal serial bus port (USB side 818, Figure 8A) and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface (USB MAC 806, Figure 8A), said on-chip Ethernet interface being connected to said Ethernet port, the said interfaces being connected to said processing circuitry for translating between Ethernet protocol data on an Ethernet bus connected to said Ethernet port and universal serial bus data for said target on-chip universal serial bus interface (cable 800, column 10, lines 47-65).

11-2. Regarding claim 2, Silverman et al. further disclose comprising an on-chip memory interface for connection to memory in said device but external to said chip (external memory interface 434, Figure 4; column 7, lines 60-64).

11-3. Regarding claim 3, Silverman et al. further disclose comprising modem circuitry for connection of a telephone line to said universal serial bus (UART 444, Figure 4; column 7, lines 45-47).

11-4. Regarding claim 4, Silverman et al. further disclose said modem circuitry comprises a soft modem (UART 444, Figure 4; column 7, lines 45-47).

11-5. Regarding claim 5, Silverman et al. further disclose said modem circuitry comprises a hard modem (modems, column 11, lines 63-65).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klaas, U.S. Patent 6,816,750 B1 issued November 9, 2004, and filed June 9, 2000, in view of Silverman et al., U.S. Patent 6,370,603 B1 issued April 9, 2002 and filed October 5, 1998.

13-1. Regarding claim 6, Klaas discloses a target integrated circuit chip (Klaas, system-on-a-chip 100, FIG. 1), said target integrated circuit chip having a digital processor (Klaas, AMR920T microprocessor core 101, FIG. 1), an on-chip emulator for controlling said digital processor and

for collecting operation data from said digital processor for communicating to off-chip circuitry (Klaas, in-circuit emulator, column 16, lines 54-65), and a target on-chip universal serial bus interface connected to said on-chip emulator (Klaas, USB host 3 ports 111, FIG. 1).

Klaas fails to expressly disclose a combination of a communication device. Nevertheless, Klaas discloses lots of interfaces for communicating with various devices.

Silverman et al. disclose a communication device comprising an Ethernet port for connection to said off-chip circuitry (Silverman, Ethernet side 814, Figure 8A), a universal serial bus port (Silverman, USB side 818, Figure 8A) and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface (Silverman, USB MAC 806, Figure 8A), said on-chip Ethernet interface being connected to said Ethernet port, the said interfaces being connected to said processing circuitry for translating between Ethernet protocol data on an Ethernet bus connected to said Ethernet port and universal serial bus data for said target on-chip universal serial bus interface (Silverman, cable 800, column 10, lines 47-65). Using the Plug-and-Play capability of USB, a cable could readily be attached and removed without requiring re-booting the machine to which the cable is attached (Silverman, column 10, lines 31-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Klaas to incorporate the teachings of Silverman et al. to obtain the invention as specified in claim 6 because using the Plug-and-Play capability of USB, a cable could readily be attached and removed without requiring re-booting the machine to which the cable is attached (Silverman, column 10, lines 31-35).

13-2. Regarding claim 7, Silverman et al. further disclose comprising modem circuitry for connection of a telephone line to said processing circuitry of said communication device (UART 444, Figure 4; column 7, lines 45-47).

14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Silverman et al., U.S. Patent 6,370,603 B1 issued April 9, 2002 and filed October 5, 1998, in view of Klaas, U.S. Patent 6,816,750 B1 issued November 9, 2004, and filed June 9, 2000.

14-1. Regarding claim 8, Silverman et al. disclose a method of communicating with a target integrated circuit chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry, and a target on-chip universal serial bus interface connected to said on-chip emulator, the method comprising:

supplying data from said off-chip circuitry via an Ethernet bus to an Ethernet port of a communication device comprising a further integrated circuit chip having on-chip Ethernet interface circuitry and on-chip processing circuitry; passing said data as an input said Ethernet interface circuitry; in said Ethernet interface circuitry, translating said data into a form suitable for said on-chip processing circuitry (Silverman, Ethernet side 814, Figure 8A);

supplying said translated data to said on-chip processing circuitry; processing said translated data to provide output data (Silverman, USB MAC 806, Figure 8A);

applying said output data to an on-chip universal serial bus interface (Silverman, USB side 818, Figure 8A).

Silverman et al. fail to expressly disclose the output data is for transfer via a universal serial bus to said on-chip emulator of said target integrated circuit chip. Nevertheless, Silverman

et al. suggest using the Plug-and-Play capability of USB, a cable could readily be attached and removed without requiring re-booting the machine to which the cable is attached (Silverman, column 10, lines 31-35).

Klaas discloses a target integrated circuit chip (Klaas, system-on-a-chip 100, FIG. 1) having a digital processor (Klaas, AMR920T microprocessor core 101, FIG. 1), an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry (Klaas, in-circuit emulator, column 16, lines 54-65), and a target on-chip universal serial bus interface connected to said on-chip emulator (Klaas, USB host 3 ports 111, FIG. 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Silverman et al. to incorporate the teachings of Klaas to obtain the invention as specified in claim 8 because using the Plug-and-Play capability of USB, a cable could readily be attached and removed without requiring re-booting the machine to which the cable is attached (Silverman, column 10, lines 31-35).

15. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Silverman et al., U.S. Patent 6,370,603 B1 issued April 9, 2002 and filed October 5, 1998, in view of Klaas, U.S. Patent 6,816,750 B1 issued November 9, 2004, and filed June 9, 2000, and further in view of Swoboda, U.S. Patent Application Publication 2002/0059541 A1, published May 16, 2002.

15-1. Regarding claim 9, Silverman et al. disclose a method comprising

providing a communication device comprising an Ethernet port (Silverman, Ethernet side 814, Figure 8A), a universal serial bus port (Silverman, USB side 818, Figure 8A) and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip

Ethernet interface and an on-chip universal serial bus interface (Silverman, USB MAC 806, Figure 8A),

Silverman et al. fail to expressly disclose (1) connecting said communication device to said target on-chip universal serial bus interface via a universal serial bus; (2) communicating data between said on-chip emulator and said on-chip processing circuitry; and (3) processing data in said on-chip processing circuitry to provide output data. Nevertheless, Silverman et al. suggest using the Plug-and-Play capability of USB, a cable could readily be attached and removed without requiring re-booting the machine to which the cable is attached (Silverman, column 10, lines 31-35).

Klaas discloses a target integrated circuit chip (Klaas, system-on-a-chip 100, FIG. 1) having a digital processor (Klaas, AMR920T microprocessor core 101, FIG. 1), an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry (Klaas, in-circuit emulator, column 16, lines 54-65), and a target on-chip universal serial bus interface connected to said on-chip emulator (Klaas, USB host 3 ports 111, FIG. 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Silverman et al. to incorporate the teachings of Klaas to obtain the invention of communicating data between a communication device and a target integrated circuit chip because using the Plug-and-Play capability of USB, a cable could readily be attached and removed without requiring re-booting the machine to which the cable is attached (Silverman, column 10, lines 31-35).

Furthermore, Silverman et al. fail to expressly disclose debugging a target integrated circuit chip using a host computer device.

Swoboda discloses a typical debug system as shown in FIG. 1. The debugger together with the on-chip trace and triggering facilities provide a means to select, record, and display chip activity of interest (Swoboda, paragraph [0061]). Specifically, Swoboda discloses:

connecting said Ethernet port to said host via an Ethernet link (Ethernet, paragraph [0065]); and

supplying said output data to said host via said Ethernet port (Ethernet, paragraph [0065]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined teachings of Silverman et al. and Klaas to incorporate the teachings of Swoboda to obtain the invention as specified in claim 9 because the communication of the disclosed debug system is typical. It is well known for one skilled in the art to obtain chip activity of interest through a typical debug system.

15-2. Regarding claims 10 and 12, Swoboda further disclose comprising loading a program from said host to said on-chip processing circuitry over said Ethernet link (Ethernet, paragraph [0065]) and running an embedded web-server process on said on-chip processing circuitry is a design choice.

15-3. Regarding claim 11, Silverman et al. disclose a method comprising

providing a communication device comprising an Ethernet port (Silverman, Ethernet side 814, Figure 8A), a universal serial bus port (Silverman, USB side 818, Figure 8A) and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip

Ethernet interface and an on-chip universal serial bus interface (Silverman, USB MAC 806, Figure 8A),

Silverman et al. fail to expressly disclose (1) connecting said communication device to said target on-chip universal serial bus interface via a universal serial bus; (2) communicating data between said on-chip emulator and said on-chip processing circuitry; and (3) processing said data in said on-chip processing circuitry to provide output data; and (4) supplying said output data to said on-chip emulator circuitry. Nevertheless, Silverman et al. suggest using the Plug-and-Play capability of USB, a cable could readily be attached and removed without requiring re-booting the machine to which the cable is attached (Silverman, column 10, lines 31-35).

Klaas discloses a target integrated circuit chip (Klaas, system-on-a-chip 100, FIG. 1) having a digital processor (Klaas, AMR920T microprocessor core 101, FIG. 1), an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry (Klaas, in-circuit emulator, column 16, lines 54-65), and a target on-chip universal serial bus interface connected to said on-chip emulator (Klaas, USB host 3 ports 111, FIG. 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Silverman et al. to incorporate the teachings of Klaas to obtain the invention of communicating data between a communication device and a target integrated circuit chip because using the Plug-and-Play capability of USB, a cable could readily be attached and removed without requiring re-booting the machine to which the cable is attached (Silverman, column 10, lines 31-35).

Furthermore, Silverman et al. fail to expressly disclose debugging a target integrated circuit chip using a host computer device.

Swoboda discloses a typical debug system as shown in FIG. 1. The debugger together with the on-chip trace and triggering facilities provide a means to select, record, and display chip activity of interest (Swoboda, paragraph [0061]). Specifically, Swoboda discloses:

connecting said Ethernet port to said host (Ethernet, paragraph [0065]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined teachings of Silverman et al. and Klaas to incorporate the teachings of Swoboda to obtain the invention as specified in claim 11 because the communication of the disclosed debug system is typical. It is well known for one skilled in the art to obtain chip activity of interest through a typical debug system.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Reference to Lehrbaum, "Embedded Systems News SOC it To 'Ya!", Linux Journal, August 2000, 2 pages, is cited as disclosing Aplio/TRIO contains CPU, Ethernet, USB interface, and software modem.

Reference to Kozu, "A 9-M Tr. Access Network System-On-a-Chip For Mega-bit Internet access at Home", Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, May 2000, pages 231-234, is cited as disclosing a system-on-a-chip solution for access network controller.

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jean R. Homere can be reached on (571) 272-3780. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day H.D.
February 22, 2005

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER